REMARKS

The Office Action dated December 16, 2002 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-14, 16-18, 24-34 are pending in the present application and submitted for consideration thereof.

CLAIM OBJECTIONS

Claims 3, 26, 29, 31 and 33 are objected to.

Claims 3, 26 and 29, 31 and 33 have been amended to address the concerns as set forth in item 4 of the Office Action. A withdrawal of the claim objections is respectfully requested.

CLAIM REJECTIONS

A.   Claims 24, 25, 27 and 28 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 24, 25, 27 and 28 have been amended to overcome this rejection by addressing the concerns as set forth in item 5 of the Office Action.

B.   Claims 1, 2, 16-18, 30, 32 and 34 are rejected under 35 U.S.C. § 102(b) as being anticipated by <u>Cocke et al.</u>, (USPN 3,577,189, "*Cocke*").

Cocke is directed to detecting a branch instruction, determining the condition specified within the branch instruction, and calculating a branch address.   Specifically,

Cocke reads an instruction corresponding to the calculated branch address and executes the instruction when an exit instruction subsequent to the branch instruction is detected.

By contrast, the present invention as set forth in claims 1, 16, 30, 32 and 34 from which claims 2, 17 and 18 directly or indirectly depend prefetches an instruction or data in accordance with an address for the instruction or an address for the data included in a pseudo instruction when it is detected and executes the prefetched instruction when a specific instruction subsequent to the pseudo instruction is detected. Accordingly, *Cocke* does not disclose the specific claimed requirement of using the pseudo instruction including an address for the instruction or an address for the data. Consequently, the present invention as recited in claims 1, 2, 16-18, 30, 32 and 34 is clearly distinguishable from *Cocke* and is not obvious over *Cocke*.

C. Claims 3-5, 9-14, 23, 26, 29, 31 and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Cocke*.

It is first noted that the rejection to claim 23 should be withdrawn in view of the cancellation thereto by the previously filed Amendment dated October 7, 2002.

Independent claims 8, 14, 31 and 33 recite the above-discussed claimed requirement of using the pseudo instruction including an address for the instruction or an address for the data, and are therefore patentable over *Cocke* for at least the reasons stated above.

As to claims 3-5, 9-13, 26 and 29, which depend directly or indirectly from claims 1 and 8, they are patentable over *Cocke* for at least the reasons stated above with respect to claims 1 and 8.
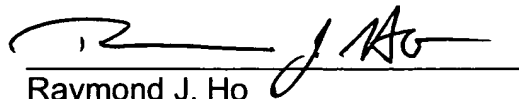
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In view of the foregoing, reconsideration of the application, withdrawal of the outstanding objections and rejections, allowance of claims 1-14, 16-18 and 24-34, and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS

1.   (Thrice Amended) A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the at least one instruction or an address for data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit;

reading the instruction or data in accordance with the address for the instruction or the address for the data with the first unit when the pseudo instruction is detected;

storing the instruction or the data in a buffer; and

executing the stored instruction with a second unit.

3.   (Twice Amended) The method of claim 1, wherein the buffer includes first and second buffers connected in parallel [with] to the memory, and the method further comprising a step of storing the instruction and data read from the memory in the first buffer and storing the instruction or data included in the detected pseudo instruction in the second buffer.

8.   (Thrice Amended) A microcontroller, comprising:

a buffer, connected to a memory, for storing instructions and data of a program read from the memory, wherein the program includes a pseudo instruction and

at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the at least one instruction or an address for data;

a first unit including,

a pseudo instruction detection unit, connected to the memory, for detecting the pseudo instruction included in the program read from the memory; and

an address control unit, connected to the external memory and the pseudo instruction detection unit, for reading the instruction or data in accordance with the address for the instruction or the address for the data when the pseudo instruction is detected and storing the instruction or the data in the buffer; and

a second unit connected to the buffer, for executing the instruction stored in the buffer.

9. (Twice Amended) The microcontroller of claim 8, wherein the buffer includes first and second buffers connected in parallel [with] to the memory, wherein the first buffer stores the instruction and data read from the memory, and the second buffer stores the instruction or data included in the detected pseudo instruction.

14. (Thrice Amended) A device for detecting a pseudo instruction present before a specific instruction, wherein the pseudo instruction includes an opcode and an operand, and wherein the device is independent of an instruction execution unit for executing the specific instruction, the device comprising:

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a detection circuit, connected to a data line, for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction; and

a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode when the pseudo instruction is detected and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for invalidating the opcode detection operation during an operand transfer period.

24. (Amended) The method of claim 1, wherein the [pseudo] at least one instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

25. (Amended) The method of claim 1, further comprising executing a no-operation (NOP) instruction [in accordance with a detection of] when the pseudo instruction is detected.

26. (Amended) The method of claim 1, further comprising [counting] the second unit ignoring an address for the pseudo instruction when receiving the address for the at least one instruction or the address for data [so that the second unit skips] to skip the pseudo instruction.

27.   (Amended)   The microcontroller of claim 8, wherein the [pseudo] at least one instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

28.   (Amended)   The microncontroller of claim 8, wherein the second unit executes a no-operation (NOP) [operation in accordance with a detection of] instruction when the pseudo instruction is detected.

29.   (Amended)   The microcontroller of claim 8, wherein the second unit [includes an address counter for counting] ignores an address for the pseudo instruction when receiving the address for the at least one instruction or the address for data [so that the second unit skips] to skip the pseudo instruction.

30.   (Amended)   A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit;

prefetching the instruction or data in accordance with the detection of the pseudo

instruction with the first unit <u>when the pseudo instruction is detected</u>; and

executing a no-operation (NOP) [operation inn accordance with the detection of]

<u>instruction when</u> the pseudo instruction <u>is detected</u> with a second unit.

31.   (Amended)   A method for prefetching instructions and data of a program

stored in a memory, wherein the program includes a pseudo instruction and at least one

instruction, the pseudo instruction being arranged before the at least one instruction and

including an address for the instruction or an address for data, the method comprising

the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit <u>when the pseudo instruction is</u>

<u>detected</u>;

prefetching the instruction or data in accordance with the detection of the pseudo

instruction with the first unit; and

[counting] <u>when receiving</u> the address for the at least one instruction or the

address for data [so that] a second unit, which is independent of the first unit, [skips]

<u>skipping</u> the pseudo instruction and [executes] <u>executing</u> the prefetched instruction.

32.   (Amended) An apparatus for prefetching instructions and data of a

program stored in a memory, wherein the program includes a pseudo instruction and at

least one instruction, the pseudo instruction being arranged before the at least one

instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit prefetches the instruction or data [in accordance with the detection of] when the pseudo instruction is detected; and

a second unit for executing a no-operation (NOP) operation in accordance with the detection of the pseudo instruction.

33.   (Amended)   An apparatus for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit prefetches the instruction or data [in accordance with the detection of] when the pseudo instruction is detected; and

a second unit for executing the prefetched instruction, wherein the second unit [includes an address unit for counting] ignores an address for the pseudo instruction when receiving the address for the at least one instruction or the address for data [so that the second unit skips] to skip the pseudo instruction.

34.   (Amended) An apparatus for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit reads the instruction or data in accordance with the address for the instruction or the address for the data when the pseudo instruction is detected, wherein the first unit includes a buffer for storing the instruction or the data; and

a second unit for executing the stored instruction.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

TANIGUCHI et al.   Art Unit: 2653

Application No.: 09/266,869   Examiner: Gautam R. Patel

Filed: March 12, 1999   Docket No.: 108075-09008

For: MICROCONTROLLER HAVING PREFETCH FUNCTION

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PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231   May 8, 2003

Sir:

Prior to initial examination of the application, please amend the above-identified

application as follows:

IN THE CLAIMS:

Please amend claims 1, 3, 8, 9, 14 and 24-34 as follows:

1.   (Thrice Amended) A method for prefetching instructions and data of a

program stored in a memory, wherein the program includes a pseudo instruction and at

least one instruction, the pseudo instruction being arranged before the at least one

instruction and including an address for the at least one instruction or an address for

data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit;